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ExaNICX40

ULTRA LOW LATENCY NETWORK INTERFACE CARD

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The ExaNIC is a 10/40Gbps PCI Express network card interface card specifically optimized for low latency environments.

While initially conceived and built for use in latency-sensitive financial applications such as high frequency trading, the ExaNIC has appeal that extends to any environment where latency is key. On an Intel Ivy Bridge test system, median latency from application to network to application is 800 nanoseconds for small packets. Half round trip TCP latencies are as low as 950 nanoseconds for small payloads.

HIGH PORT DENSITY

Dual QSFP+ ports in a half height form factor provide eight 10GbE interfaces

Tthe ExaNIC X40 can connect to eight SFP+ ports QSFP+ breakout cables and/or Layer 1 switches. This enables a range of high performance applications such as packet capture across multiple connections, or market data line arbitration across many different feeds.

EASY TO USE

In addition to a standard Linux driver, a transparent TCP and UDP acceleration library is included, as well as a library for low-level access.

A transparent socket acceleration library allows applications to benefit from the low latency of kernel bypass, in most cases without modifications to the applications. For the most latency sensitive applications, a library called 'libexanic' allows direct low-level access to the ExaNIC hardware and includes simple functions for sending and receiving Ethernet frames. With the optional firmware development kit, it is even possible to extend the ExaNIC firmware and add your own logic to the onboard FPGA.

ADVANCED CAPTURE

Flow steering delivers packets to the right application's receive buffer.

Filters can be defined over Ethernet frame components such as SRC/DST MAC, SRC/DST IP etc, and a receive buffer associated with that filter. As packets come off the wire, the ExaNIC will analyze the traffic and deliver packets the match filters directly to the correct receive buffer. Non-matched packets are delivered to the default buffer. This flow steering is done inline at line rate, adding no additional latency. Flow hashing distributes packets evenly across multiple buffers, allowing CPU load to be spread for demanding capture and analysis applications.

TIMESTAMPING

Built-in timestamping functionality records each frame's arrival time to within 6.2ns.

These timestamps are available through a direct API and through Exact Capture, our free and open source, high-rate capture system. Exact Capture can write tcpdump-compatible captures at line-rate to disk. Additionally, the ExaNIC X40 features a Pulse-Per-Second (PPS) input and output and supports hardware accelerated PTP. These can be used to synchronize the ExaNIC clock to external time references (such as a GPS receivers) allowing users to meaningfully compare captured timestamps across multiple servers and geographic locations.

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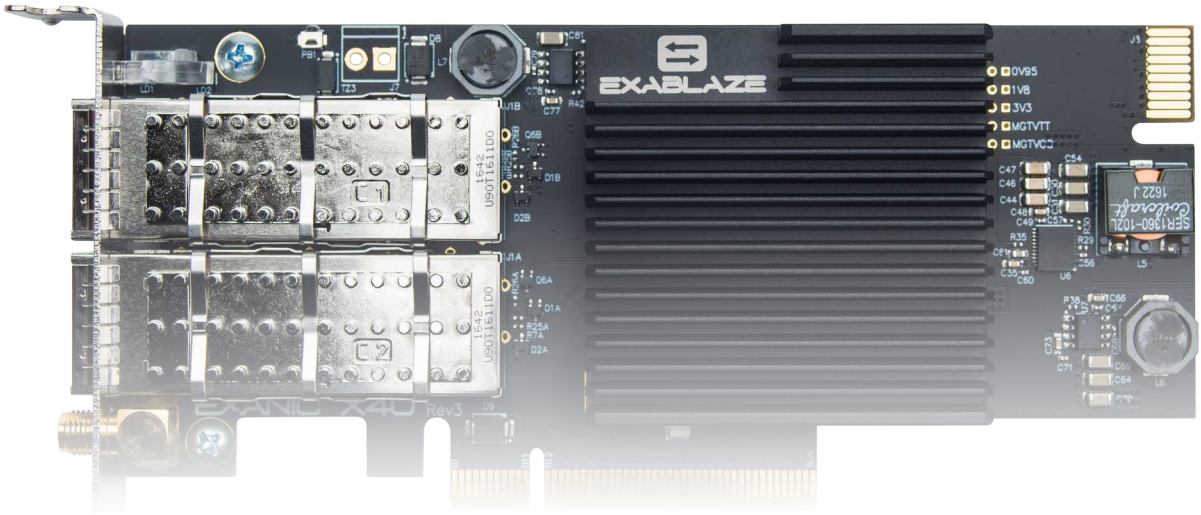

PERFORMANCE

Typical latency, raw frames: (See Note 1)
- 60 bytes: 800 ns
- 300 bytes: 1.02 µs

Typical latency, raw frames with preloaded TX buffer: (See Note 1)
- 60 bytes: 730 ns
- 300 bytes: 950 ns

Typical latency, UDP: (See Note 2)
- 14 bytes: 900 ns
- 300 bytes: 1.22 µs

Typical Latency, TCP: (See Note 2)
- 14 bytes: 950 ns
- 300 bytes: 1.22 µs

TIMESTAMPING

Timestamp resolution:
- 6.2ns

Timestamp availability:
- all received frames, most recent transmitted frame

Time synchronization:
- Host, hardware assisted PTP, optional PPS

PPS input/output:
- 3.3V CMOS, selectable 50ohm termination

GENERAL

Form factor:
- Low profile PCI Express Card
- 150x68mm (5.9x2.67in)

Ports:
- 2 QSFP+
- SMA for PPS in/out

Data rates:
- 40GbE, 10GbE, 1GbE, 100M Fast Ethernet

Supported Media:
- Fiber (10GBASE-SR, 10GBASE-LR, 1000BASE-SX), SFP+ Direct Attach

Host Interface:
- PCIe x8 Gen 3 @ 8.0 GT/s per lane

Operating Systems:
- Linux x86_64 (all distributions)
- Windows

OTHER FEATURES

Flow steering:
- 128 IP rules per port
- 64 MAC rules per port

Capture:
- Line rate capture to disk

FPGA Development Kit:
- Add custom user logic to FPGA
- Xilinx Ultrascale XCKU035-2
- Fully integrated with drivers, utilities & TCP/UDP stack

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Notes

1. Latencies are median latencies for raw frames from wire-userspace-wire via the libexanic library, on a 3.5Ghz Intel Ivy Bridge processor.
2. Latencies are median half round trip time latencies for the sockperf benchmark using the exasock socket Acceleration Library. More information about benchmarking methodology is available on request.