EXABLAZE
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ExaNICX25

ULTRA LOW LATENCY NETWORK INTERFACE CARD

FASTEST EXANIC EVER BUILT

The ExaNIC X25 is specifically optimized for low latency operation.

It features software trigger-to-response latencies as low as **568ns**. This is up to **20%** faster than previous ExaNIC models, making it the fastest ExaNIC ever built. Users will find this drop-in replacement NIC accelerates tick-to-trade performance to previously unachievable speeds, increasing the efficacy and profitability of software based trading systems.

ADVANCED SOFTWARE PROGAMABILITY

The ExaNIC X25 provides the most powerful programmable software interface on the market.

Programability features include:

- **Zero Cost Hardware Flow Steering** - allowing users to steer and pre-filter important traffic to the right memory and CPU core at no latency penalty.
- **Cut-Though Receive** – this patented mechanism allows software to process packet fragments as they arrive from the wire, while packet tails are still in flight. This is especially effective for slow line speeds (e.g. 1GbE). The ExaNIC X25 software API puts users well ahead of traditional store-and-forward NIC designs to make better decisions, faster.
- **ExaSOCK TCP/IP Acceleration** - Unmodified sockets applications can benefit from the speed and power of the ExaNIC X25 using ExaSOCK. ExaSOCK is an in-place TCP/IP sockets acceleration system. ExaSOCK's Extension API allows it to seamlessly interoperate with the X25's Transmit Preloading featuture described below.
- **Pre-loaded packet transmit** - The ExaNIC X25 allows users to preload transmit frames, saving 60ns from the transmit path. The X25 features enlarged packet transmit buffers allowing many more frames to be preloaded, leading to more versatile transmission choices.
- **High resolution timestamps** – 4ns timestamps are applied to every received packet and the most recently transmitted packet. The X25 also features out of the box support for IEEE1588 (PTP) and high-speed capture to disk using free and open source Exact-Capture software.

25GBE READY

The ExaNIC X25 is a pure FPGA based network adapter that is 25GbE ready.

FPGA network adapters extend the useful life of the device by allowing new features and speed enhancements to be downloaded into the device after deployment. For example, the ExaNIC X25 will support 25G Ethernet speeds through a firmware update. This will reduce capital expenditure on lengthy and difficult infrastructure upgrades.

ALL FPGA DESIGN

The ExaNIC X25 is built using the latest generation Xilinx Ultrascale+ FPGA

It optionally ships with 4GB of DDR4 memory for custom use. It is a compact adapter in low-profile form-factor. Users can benefit from the pure FPGA design by offloading critical network processing functions directly into the NIC, while maintaining the ease of use and administration of a production grade network adapter.

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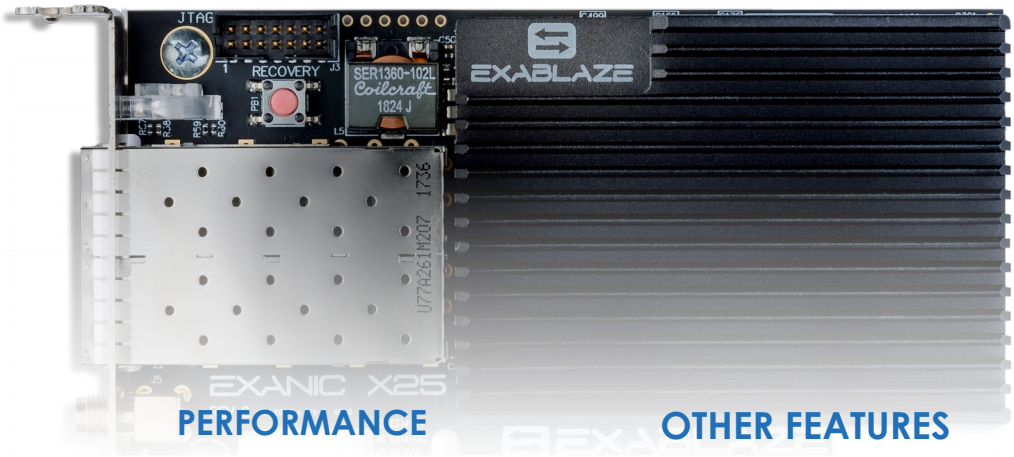

PERFORMANCE

Typical latency, raw frames: (See Note 1)
- 64 bytes: 696 ns
- 256 bytes: 897 ns

Typical latency, raw frames with preloaded TX buffer: (See Note 1)
- 64 bytes: 629 ns
- 256 bytes: 665 ns

Typical latency, UDP: (See Note 2)
- 14 bytes: 810 ns
- 256 bytes: 1.1 µs

Typical Latency, TCP: (See Note 2)
- 14 bytes: 850 ns
- 256 bytes: 1.1 µs

TIMESTAMPING

Timestamp resolution:
- 4ns

Timestamp availability:
- all received frames, most recent transmitted frame

Time synchronization:
- Host, hardware assisted PTP, optional PPS

PPS input/output:
- 3.3V CMOS, selectable 50ohm termination

OTHER FEATURES

Capture:
- Line rate capture to disk

Flow steering:
- 128 IP rules per port
- 64 MAC rules per port

FPGA Development Kit:
- Add custom user logic to FPGA
- 4GB DDR 4
  Xilinx Ultrascale XCKU3P-2
- Fully integrated with drivers, utilities & TCP/UDP stack

GENERAL

Form factor:
- Low profile PCI Express Card
- 117x68mm (4.65x2.67in)

Ports:
- 2x SFP28
- SMA for PPS in/out

Data rates:
- 25GbE[3], 10GbE, 1GbE, 100M Fast Ethernet

Supported Media:
- Fiber (25GBASE-SR, 25GBASE-LR,25GBASE-CR), SFP(+/28) Direct Attach

Host Interface:
- PCIe x8 Gen 3 @ 8.0 GT/s per lane

Operating Systems:
- Linux x86_64 (all distributions)
- Windows

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Notes

1. Latencies are median latencies for raw frames from wire-userspace-wire via the libexanic library, on a 3.5Ghz Intel Ivy Bridge processor.
2. Latencies are median half round trip time latencies for the sockperf benchmark using the exasock socket acceleration library. More information about benchmarking methodology is available on request.
3. Hardware is built and tested at 25Gbs. 25GbE supported with a future firmware update.