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ExaNICX10

ULTRA LOW LATENCY NETWORK INTERFACE CARD

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The ExaNIC is a 10Gbps PCI Express network card interface card specifically optimized for low latency environments.

While initially conceived and built for use in latency-sensitive financial applications such as high frequency trading, the ExaNIC has appeal that extends to any environment where latency is key. On an Intel Ivy Bridge test system, median latency from application to network to application is 780 nanoseconds for small packets, which is significantly better than competing network cards on the same hardware. Half round trip TCP latencies are as low as 930 nanoseconds for small payloads.

EASY TO USE

In addition to a standard Linux driver, a transparent TCP and UDP acceleration library is included, as well as a library for low-level access.

A transparent socket acceleration library allows applications to benefit from the low latency of kernel bypass, in most cases without modifications to the applications. For the most latency sensitive applications, a library called 'libexanic' allows direct low-level access to the ExaNIC hardware and includes simple functions for sending and receiving Ethernet frames. With the optional firmware development kit, it is even possible to extend the ExaNIC firmware and add your own logic to the onboard FPGA.

ADVANCED CAPTURE AND TIMESTAMPING

Built-in timestamping functionality records each frame's arrival time to within 6.2ns.

These timestamps are available through a direct API and through Exact Capture, our free and open source, high-rate capture system. Exact Capture can write tcpdump-compatible captures at line-rate to disk. Additionally, the ExaNIC has a Pulse-Per-Second (PPS) input and output and supports hardware accelerated PTP. These can be used to synchronize the ExaNIC clock to external time references (such as a GPS receivers) allowing users to meaningfully compare captured timestamps across multiple servers and geographic locations. Finally, flow steering can be used to deliver packets to the right application's receive buffer, while flow hashing can be used to distribute packets across multiple CPU cores for demanding capture applications.

BUILT–IN BRIDGING

The ExaNIC includes integrated support for bridging, which can further reduce latency by hundreds of nanoseconds.

Normally sharing an upstream connection between multiple servers would necessitate introducing a switch. The bridging feature allows the most latency critical server to be directly connected to the upstream connection. Packets not destined for the local server can be bridged to the second port, transparently and with low latency. This port could be connected to a backup server or to a downstream switch.

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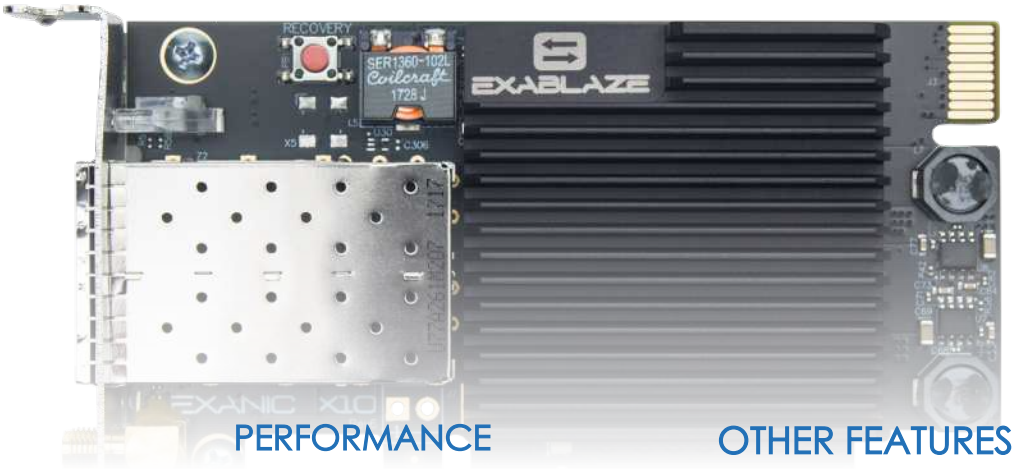

PERFORMANCE

Typical latency, raw frames: (See Note 1)
- 60 bytes: 780 ns
- 300 bytes: 1 µs

Typical latency, raw frames with preloaded TX buffer: (See Note 1)
- 60 bytes: 710 ns
- 300 bytes: 930 ns

Typical latency, UDP: (See Note 2)
- 14 bytes: 880 ns
- 300 bytes: 1.2 µs

Typical Latency, TCP: (See Note 2)
- 14 bytes: 930 ns
- 300 bytes: 1.2 µs

TIMESTAMPING

Timestamp resolution:
- 6.2ns

Timestamp availability:
- all received frames, most recent transmitted frame

Time synchronization:
- Host, hardware assisted PTP, optional PPS

PPS input/output:
- 3.3V CMOS, selectable 50ohm termination

OTHER FEATURES

Bridging:
- Optional forwarding between ports 1 and 2, latency <110ns

Capture:
- Line rate capture to disk

Flow steering:
- 128 IP rules per port
- 64 MAC rules per port

FPGA Development Kit:
- Add custom user logic to FPGA
- Xilinx Ultrascale XCKU035-2
- Fully integrated with drivers, utilities & TCP/UDP stack

GENERAL

Form factor:
- Low profile PCI Express Card
- 117x68mm (4.65x2.67in)

Ports:
- 2 SFP+
- SMA for PPS in/out

Data rates:
- 10GbE, 1GbE, 100M Fast Ethernet

Supported Media:
- Fiber (10GBASE-SR, 10GBASE-LR, 1000BASE-SX), SFP+ Direct Attach

Host Interface:
- PCIe x8 Gen 3 @ 8.0 GT/s per lane

Operating Systems:
- Linux x86_64 (all distributions)
- Windows

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Notes

1. Latencies are median latencies for raw frames from wire-userspace-wire via the libexanic library, on a 3.5Ghz Intel Ivy Bridge processor.
2. Latencies are median half round trip time latencies for the sockperf benchmark using the exasock socket acceleration library. More information about benchmarking methodology is available on request.